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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,925	07/24/2000	Yong jin Park	9898-156	4905

7590 08/27/2003

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EXAMINER
NGUYEN, MIKE

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,925	PARK ET AL.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's amendment file on 06/11/2003 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-18 are pending for the examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Roohparvar (U.S. Pat. No. 5,526,364).

5. As to claim 1, Roohparvar teaches a semiconductor memory device (see figure 1), comprising:

a first plurality of external signals (see figure 1 elements 11, 12 and column 3 lines 6-15);

a second plurality of externals (see figure 1 elements CE bar, 17 and column 3 lines 6-16);

a mode set circuit adapted to operate in at least a test and normal modes and generate plurality of mode signals (see figure 1 and column 2 lines 56-67);

where during the test mode, the first plurality of external of external signals have a voltage level higher than a power supply voltage (see column 2 lines 56-67 and column 3 lines 7-15);

6. As to claim 17, Roohparvar teaches the semiconductor memory device of claim 1 where the voltage level higher than the power supply voltage is supplied only for a short period of time (see column 2 lines 62-64 wherein the voltage level higher than the power supply voltage is supplied while in a test mode).

7. As to claim 18, Roohparvar teaches the semiconductor memory device of claim 1

where the mode set circuit operates responsive only to the first plurality of external signals (see column 2 lines 57-67 and column 3 lines 7-15); and

where during the normal mode, the mode set circuit operates responsive only to the second plurality of external signals (see column 3 lines 40-42 wherein if one of the first plurality of external signals drops below a predetermined voltage then the test mode will be disabled and the mode set circuit operates responsive only to second plurality of external signals).

8. As to claim 3, Roohparvar teaches a semiconductor memory device (see figure 1), comprising:

a first plurality of pads adapted to receive a corresponding plurality of first external signals (see figure 1 elements 11-14 and column 2 lines 57-67 and column 3 lines 7-15);

a second plurality of pads adapted to receive a corresponding plurality of second external signals (see figure 1 elements CE bar, 17, 18, 10 and column 2 lines 57-67 and column 3 lines 7-15); and

an input and output mode set circuit coupled to the first and second plurality of pads and adapted to generate a plurality of input and output mode signals responsive to the plurality of first and second external signals (see figure 1 and column 3 lines 7-15);

wherein, during a test mode, the input and output mode set circuit is adapted to generate

the plurality of input and output mode signals responsive only to the plurality of first external signals, the plurality of the first pads receiving a high voltage higher than a voltage level of a power supply signal thereby generating a plurality of first external signals having a level higher than a voltage level of the power supply signal (see column 2 lines 56-67 and column 3 lines 7-15);

wherein, during normal operations, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to the plurality of second external signals (see column 3 lines 40-42 wherein if one of the first plurality of external signals drops below a predetermined voltage then the test mode will be disabled and the mode set circuit operates responsive to second plurality of external signals).

wherein the high voltage is applied to the plurality of first pads only for a short period of time (see column 2 lines 62-64 wherein the voltage level higher than the power supply voltage is supplied while in a test mode).

9. As to claim 5, Roohparvar teaches the semiconductor memory device of claim 3 wherein the supply signal is applied to the semiconductor memory device after the high voltage is applied to one of the first plurality of pads (see column 3 lines 7-43).

10. As per claims 6 and 11, Roohparvar teaches the semiconductor memory device of claim 3 and claim 10 wherein the plurality second pads float (see figure 1 elements CE bar, 17 wherein the plurality second pads is not connect each other)

11. As per claims 7 and 12, Roohparvar teaches the semiconductor memory device of claim 3 and 12 wherein at least one of the plurality of pads is grounded to a ground terminal of the

semiconductor memory device (it is inherently at least one of the plurality of pads is grounded to a ground terminal of semiconductor memory device).

12. As to claim 8, Roohparvar teaches the semiconductor memory device of claim 3 wherein the input and output mode set circuit comprises:

a pad circuit coupled to the first plurality of pads and adapted to generate a plurality of first signals, one of the plurality of first signals being active when the high voltage is applied to at least one of the plurality of pads (see figure 1 elements 11, 12 and column 3 lines 7-43);

a control signal generating circuit adapted to generate a plurality of control signal responsive to the plurality of first signals and a plurality of second signals (see column 3 lines 7-43); and

an input and output mode signal generating circuit adapted to generate the plurality of input and output mode signals responsive to the plurality of control signals and the plurality of second external signals (see column 3 lines 7-43).

13. As to claim 9, Roohparvar teaches the semiconductor memory device of claim 8 wherein the plurality of second signals comprises a power supply sense signal activated when the power supply signal has a level equal to or greater than a predetermined level and input and output mode control signal activate responsive to a write enable signal, a row address strobe signal, and a column address strobe signal (see column 3 lines 32-43).

14. As to claim 10, Roohparvar teaches a semiconductor memory device, comprising:

a plurality of pads for receiving a corresponding plurality of external signals (see figure 1 elements CE bar, 11-12, 17); and

an input and output mode set circuit coupled to the plurality of pads and adapted to

generate a plurality of input and output mode signals (see figure 1 and column 3 lines 7-43);

wherein, during a test mode, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to plurality of mode register address signals (see column 3 lines 7-32);

wherein, during normal mode operation, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to the plurality of external signals received at the plurality of pads (see column 3 lines 33-43); and

wherein the input and output mode set circuit includes:

a mode register set circuit adapted to receive a group of the plurality of mode register address signals and first and second internal signals and adapted to generate first and second mode register signals responsive to the group of mode register address signals and the first and second internal signals (see column 3 lines 7-43);

a control signal generating circuit adapted to generate a plurality of control signal responsive to the first and second mode register signals, a remaining group of the plurality of mode register address signals, the first internal signal, and a third internal signal (see column 3 lines 7-43); and

an input and output mode signal generator adapted to receive the plurality of control signals, cut off signals the plurality of external control signals responsive to at least one of the plurality of control signal, and generate the plurality of input and output mode signals responsive to remaining control signals (see column 3 lines 7-43).

15. As to claim 14, Roohparvar teaches the semiconductor memory device of claim 13 wherein the first internal signal is a power supply sense signal enabled when a power supply has

a level equal to or greater than a predetermined level and internal signal is enabled when a write enable signal, a row address strobe signal, and a column address strobe signal (see column 3 lines 32-43).

16. As to claim 15, Roohparvar teaches the semiconductor memory device of claim 13 wherein, during the normal operation, the second mode register signal and the first and second internal signals are deactivated thereby deactivating the first, second, and third control signals and wherein the input and output mode signal generating circuit is adapted circuit is adapted to generate the input and output mode signals responsive to the plurality of external signals (see column 3 lines 32-42).

17. As to claim 16, Roolparvar teaches the semiconductor memory device of claim 10 wherein the plurality of pads includes two pads (see figure 1 elements 11, 12).

Response to Arguments

18. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,177,745 (Rozman)

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

Mike Nguyen
Patent Examiner
Group Art Unit 2182

01/24/2003

KIM HUYNH
PRIMARY EXAMINER 8/25/03